cg

UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/833,578	04/13/2001	Joel Zvi Apisdorf	ACRN-002/00US	5625

26384	7590	01/14/2005

NAVAL RESEARCH LABORATORY
ASSOCIATE COUNSEL (PATENTS)
CODE 1008.2
4555 OVERLOOK AVENUE, S.W.
WASHINGTON, DC 20375-5320

EXAMINER
TSAI, HENRY

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)
Office Action Summary		09/833,578	APISDORF ET AL.
		Examiner	Art Unit
		Henry W.H. Tsai	2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8/23/01*.

2a)☐ This action is **FINAL.**   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

    4a) Of the above claim(s) __ is/are withdrawn from consideration.

5)☒ Claim(s) *1-45* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: _____.

DETAILED ACTION

Specification

1.   The disclosure is objected to because of the following

informalities: at page 34, line 4, "904A" should read –902A–.

Appropriate correction is required.

Claim Objections

2.   Claims 11, 36, and 41 are objected to because of the

following informalities:

In clam 11, line 2, before "memory", -a- should be

inserted;

In clam 36, line 2, before "memory", -a- should be

inserted; and

In clam 41, line 2, before "memory", -a- should be

inserted.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3.   The following is a quotation of the second paragraph of 35

U.S.C. 112:

> The specification shall conclude with one or more claims particularly
> pointing out and distinctly claiming the subject matter which the applicant
> regards as his invention.

4.   Claims 15, and 20 are rejected under 35 U.S.C. 112, second

paragraph, as being indefinite for failing to particularly point

out and distinctly claim the subject matter which applicant

regards as the invention.

In claim 15, "said update generator" lacks proper

antecedent basis since it was not mentioned previously in the

claims.

In claim 20, "said update generator" lacks proper

antecedent basis since it was not mentioned previously in the

claims.

Applicant is required to review the claims and correct all

language which does not comply with 35 U.S.C. § 112, second

paragraph.

Claim Rejections - 35 USC § 102

5.   The following is a quotation of the appropriate paragraphs

of 35 U.S.C. 102 that form the basis for the rejections under

this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or
a foreign country or in public use or on sale in this country, more than one
year prior to the date of application for patent in the United States.

6.   Claims 1-45 are rejected under 35 U.S.C. 102(b) as being

anticipated by Olnowich (U.S. Patent No. 6,044,438) (hereafter

referred to as Olnowich'438).

Referring to claim 1, Olnowich'438 discloses, as claimed,

an apparatus (see Figs. 1A and 1B) for forwarding data between

processing elements, comprising: a first processing element (34

node in other network, see Fig. 1A), said first processing

element including an update-transmit element (SEND ADAPTER 14,

see Fig. 1B, note node 34 in other network comprises the

elements same as that shown in Fig. 1B for node 30); a

forwarding storage element (SEND FIFO 40, 41, or 42, see Fig.

1B) coupled to said update-transmit element (SEND ADAPTER 14,

see Fig. 1B, note node 34 in other network comprises the

elements same as that shown in Fig. 1B for node 30); and a

second processing element (30, the node shown in Fig. 1B)

coupled to said forwarding storage element, said second

processing element including: a register (such as data register

602, or 604, see Fig. 15D), and an address register (such as

691, 692, 693, or 694, see Fig. 18A).

Referring to claim 14, Olnowich'438 discloses, as claimed,

an apparatus (see Figs. 1A and 1B) for forwarding data between

processing elements, comprising: a first processing element (30,

the node shown in Fig. 1B) including an address register (such

as 691, 692, 693, or 694, see Fig. 18A), a first memory address

(the address in 826 B, see Fig. 18A) being stored in said

address register; a forwarding storage element (SEND FIFO 40,

41, or 42, see Fig. 1B) coupled to said first processing

element: and a second processing element (34 node in other

network, see Fig. 1A) coupled to said forwarding storage element

(SEND FIFO 40, 41, or 42, see Fig. 1B), said second processing

element (34 node in other network, see Fig. 1A) transmitting a

second memory address (the address in 826A, see Fig. 18A) to

said forwarding storage element, said forwarding storage element

(SEND FIFO 40, 41, or 42, see Fig. 1B) transmitting the second

memory address (the address in 826A, see Fig. 18A) to said first

processing element (30, the node shown in Fig. 1B); said first

processing element (30, the node shown in Fig. 1B) comparing (by

using COMPARE 800A-800D, see Fig. 18A) the second memory address

(the address in 826A, see Fig. 18A) with the first memory

address (the address in 826 B, see Fig. 18A).

Referring to claim 31, Olnowich'438 discloses, as claimed, a

method (see Figs. 1A and 1B) for reducing data retrieval,

latencies in a multiple processing element environment,

comprising: receiving (through RECEIVE ADAPTER 12 and RECEIVE

FIFO, 44-46, see Fig. 1B), at a first processing element (30,

the node shown in Fig. 1B), update data (the data send from node

34) forwarded from a second processing element (34 node in other

network, see Fig. 1A), the update data including data relating

to operations performed at the second processing element;

retrieving (the processor 50 (note the second processing

element, node 34 in other network, see Fig. 1A and the first

processing element, node 30, share the memory 54, see Fig. 1B,

and see col. 11, lines 14-16, the nodes are tightly

coupled) retrieves and uses the received data through data bus

see Fig. 2A) data from the update data in order to execute an

instruction at the first processing element (as set forth above,

the second processing element, node 34 in other network, see

Fig. 1A and the first processing element, node 30, share the

memory 54, see Fig. 1B, and see col. 11, lines 14-16, the nodes

are tightly coupled); and revising (such as the data in shared

memory 54 are to be revised after execution in processor 50 of

node 30) a subset of the received update data in response to the

execution of the instruction on the first processing element

(30, the node shown in Fig. 1B).

Referring to claim 39, Olnowich'438 discloses, as claimed, a

method (see Figs. 1A and 1B) for forwarding data between

processing elements, comprising: storing first memory address

(the address in 826B, see Fig. 18A) to an address register (such

as 691, 692, 693, or 694, see Fig. 18A) at a first processing

element (30, the node shown in Fig. 1B); retrieving a second

memory address (the address in 826A, see Fig. 18A) associated

with a second processing element (34 node in other network, see

Fig. 1A) from a forwarding storage element (SEND FIFO 40, 41, or

42, see Fig. 1B); comparing (by using COMPARE 800A-800D, see

Fig. 18A) the second memory address with the first memory

address; and updating a data register (such as data register

602, or 604, see Fig. 15D) at the first processing element (30,

the node shown in Fig. 1B) with a data value from the second

processing element (34 node in other network, see Fig. 1A) in

response to said comparing.

As to claims 2 and 16, Olnowich'438 also discloses: said

forwarding storage element (SEND FIFO 40, 41, or 42, see Fig.

1B) is a first-in first-out storage element.

As to claims 3 and 17, Olnowich'438 also discloses: said

forwarding storage element (SEND FIFO 40, 41, or 42, see Fig.

1B) is a queue.

As to claim 4, Olnowich'438 also discloses: said forwarding storage element (<u>SEND FIFO 40, 41, or 42, see Fig. 1B</u>) receives a first memory address (<u>the address in 826A, see Fig. 18A</u>) from said update-transmit element (<u>SEND ADAPTER 14, see Fig. 1B, note node 34 in other network comprises the elements same as that shown in Fig. 1B for node 30</u>) and said second processing element (<u>30, the node shown in Fig. 1B</u>) compares (<u>by using COMPARE 800A-800D, see Fig. 18A</u>) the first memory address (<u>the address in 826A, see Fig. 18A</u>) in said forwarding storage element with a second memory address (<u>the address in 826B, see Fig. 18A</u>) in said address register (<u>such as 691, 692, 693, or 694, see Fig. 18A</u>).

As to claims 5 and 19, Olnowich'438 also discloses: said second processing element stores data from said forwarding storage element to the register of said second processing element based on the comparison of the second memory address with the first memory address (<u>see Col. 28, lines 48-55. Also note the remote store is based on the address comparison by COMPARATOR 650, see Fig. 15B</u>).

As to claims 6 and 21, Olnowich'438 also discloses: said first processing element and said second processing element is disposed within a telecommunications switch (<u>see switch interconnection network 20 in Fig. 1A</u>).

As to claim 7, Olnowich'438 also discloses: said second
processing element stores data from said update-transmit element
to the register of said second processing element (note this is
the situation when the remote store request is sent from the
first processing element and based on the address comparison by
COMPARATOR 650, see Remote read/store message generation 630 in
Fig. 15B).

As to claims 8, 15, and 22, Olnowich'438 also discloses:
said forwarding storage element (SEND FIFO 40, 41, or 42, see
Fig. 1B) includes a data field (such as data fields for WORW
COUNT 819 or MEMORY AREA 815 inside message header 128A, see
Fig. 7) and an address field (such as memory address field 818,
see also col. 36, lines 49-50).

As to claims 9 and 23, Olnowich'438 also discloses: said
forwarding storage element (SEND FIFO 40, 41, or 42, see Fig.
1B) includes a last-update flag (certainly a last-update flag is
used in the FIFO replacement algorithm).

As to claims 10 and 24, Olnowich'438 also discloses: said
forwarding storage element includes a time-to-live field (TIME
STAMP filed 817 inside message header 128A, see Fig. 7, see also
col. 36, lines 49-55).

As to claim 11, Olnowich'438 also discloses: said first
processing element writes the data to memory (such as the shared

memory 54, see Fig. 1B) shared by said first processing element

and said second processing element.

As to claims 12, Olnowich'438 also discloses: a shared

memory (such as the shared memory 54, see Fig. 1B).

As to claims 13, 30, 38, and 45, Olnowich'438 also

discloses: a third processing element (another node 34 in

another network, see Fig. 1A) coupled to said first processing

element (34 node in other network, see Fig. 1A), said first

processing element sending a signal (such as ACCEPT control

signal in 61 as shown in Fig. 3) to said third processing

element indicating that said third processing element may access

a memory (54, see Fig. 1B) shared between said first processing

element and said third processing element (note the first

processing element, node 34 in other network, see Fig. 1A and

the third processing element, another node 34, share the memory

54, see Fig. 1B, col. 8, lines 8-16, and col. 11, lines 14-16,

the nodes are tightly coupled).

As to claim 18, Olnowich'438 also discloses: said first

processing element (30, the node shown in Fig. 1B) includes a

data register (such as data register 602, or 604, see Fig. 15D),

said first processing element (30, the node shown in Fig. 1B)

storing data associated with a memory address (the address in

826A, see Fig. 18A) from said forwarding storage element to said

data register (such as data register 602, or 604, see Fig. 15D).

As to claim 20, Olnowich'438 also discloses: as best

understood, said update generator transmits a data value (word

count 819, see Fig. 7) and associated memory address (memory

address 818, see Fig. 7) to said forwarding storage element

As to claim 25, Olnowich'438 also discloses: said first

processing element (30, the node shown in Fig. 1B) includes said

forwarding storage element (SEND FIFO 40, 41, or 42, see Fig.

1B).

As to claim 26, Olnowich'438 also discloses: said second

processing element (node 34 in other network) includes said

forwarding storage element (SEND FIFO 40, 41, or 42, see Fig.

1B). Note node 34 in other network comprises the elements same

as that shown in Fig. 1B for node 30.

As to claim 27, Olnowich'438 also discloses: said forwarding

storage element (SEND FIFO 40, 41, or 42, see Fig. 1B) is

separate from said first processing element and said second

processing element. Note node 34, different from nodes 30 and

34 set forth above, in another network comprises the elements,

such as SEND FIFO 40, 41, or 42, see Fig. 1B same as that shown

in Fig. 1B for node 30.

As to claim 28, Olnowich'438 also discloses: said first

processing element and said second processing element are

included in a ring of processing elements (since a plurality of

nodes 39, and 34 communicate via messages sent over an switch

interconnection network 20 in Fig. 1A certainly will be disposed

in a ring).

As to claim 29, Olnowich'438 also discloses: said first

processing element is adjacent to said second processing element

in a ring of processing elements (since a plurality of nodes 39,

and 34 communicate via messages sent over an switch

interconnection network 20 in Fig. 1A).

As to claim 32, Olnowich'438 also discloses: forwarding the

revised subset of the update data a third processing element

(note this is the situation when the remote store/read request

is sent from the first processing element or the second

processing element, see Remote read/store message generation 630

in Fig. 15B).

As to claim 33, Olnowich'438 also discloses: forwarding a

subset of the received update data to a third processing element

(note as set forth above, this is the situation when the remote

store/read request is sent from the first processing element or

the second processing element, see Remote read/store message

generation 630 in Fig. 15B).

As to claim 34, Olnowich'438 also discloses: generating update data at the second processing element, and forwarding the generated update data to a third processing element (note as set forth above, this is the situation when the remote store/read request is sent from the second processing element after the execution thereof, see Remote read/store message generation 630 in Fig. 15B).

As to claim 35, Olnowich'438 also discloses: the update data is associated with a variable (such as the variable inside the shared memory 54, see Fig. 1B) shared by the first processing element and the second processing element.

As to claim 36, Olnowich'438 also discloses: the update data includes a memory address that is associated with memory (the shared memory 54, see Fig. 1B) shared by the first processing element and the second processing element.

As to claim 37, Olnowich'438 also discloses: decrementing a time-to-live value associated with the data value (best reasonably and broadly interpreted, since the time stamp 817 is related to the order of the time).

As to claim 40, Olnowich'438 also discloses: the data value is associated with a shared variable (in the shared memory 54, see Fig. 1B, and see also col. 11, lines 14-16).

As to claim 41, Olnowich'438 also discloses: the first

memory address and the second memory address are associated with

memory (the shared memory 54, see Fig. 1B, and see also col. 11,

lines 14-16) shared by the first processing element and the

second processing.

As to claim 42, Olnowich'438 also discloses: identifying a

validity (see v bits in 660A-660H, see Fig. 16, or v bits in

699A-699D, see Fig. 18A) of the data value.

As to claim 44, Olnowich'438 also discloses: the data value

is associated with a particular network connection record (see

Fig. 7, regarding destination node ID is contained in the

message header 128B, and the specific nodes are related to a

particular network connection).

Conclusion

7.   The prior art made of record and not relied upon is

considered pertinent to applicant's disclosure. Gove'083

discloses Reconfigurable multi-processor operating in SIMD mode

with one processor fetching instructions for use by remaining

processors. The crossbar switch serves to establish the

processor memory links and an inter-processor communication link

allows the processors to communicate with each other for the
purpose of establishing operational modes. Wilkinson et al.'915
discloses a SIMIMD array processing system. A partitionable
section of the array containing several processing units are
contained on a silicon chip arranged with "pickets", elements of
the processing array, each preferably consisting of combined
processing element with a local memory for processing bit
parallel bytes of information in a clock cycle. Reckhter'841
discloses a technique for handling forwarding transients with
link state routing protocol. As shown in Fig. 6, the packet may
be forwarded over the path to the destination in Step 610 but
only after decrementing a time-to-live or lifetime entry of a
conventional network layer header of the packet (Step 608).

Contact Information

8.   Any inquiry concerning this communication or earlier
communications from the examiner should be directed to Dr. Henry
Tsai whose telephone number is (571) 272-4176. The examiner can
normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM.
If attempts to reach the examiner by telephone are unsuccessful,
the examiner supervisor, Eddie Chan, can be reached on (571)

272-4162. Any inquiry of a general nature or relating to the

status of this application or proceeding should be directed to

the TC central telephone number, (571) 272-2100.

9.   In order to reduce pendency and avoid potential delays,

Group 2100 is encouraging FAXing of responses to Office actions

directly **into the Group at fax number: 703-872-9306.** This

practice may be used for filing papers not requiring a fee. It

may also be used for filing papers which require a fee by

applicants who authorize charges to a PTO deposit account.

Please identify the examiner and art unit at the top of your

cover sheet. Papers submitted via FAX into Group 2100 will be

promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER

January 10, 2005